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LA C5

Process Technology
LA C5: 0.5µm Process Technology

Overview

The LA C5 process family from LA Semiconductor is designed to support medium density, high performance mixed signal designs. Built in the former AMI/onsemi 200mm factory in Pocatello, Idaho, LA C5 has similar performance to the onsemi C5 process but is enhanced to allow up to 5 metal levels and has improved Poly/Poly capacitor lifetimes.

Features

- 2-5 Metal layers
- Poly to Poly Capacitors with improved lifetime
- EEPROM
- Schottky Diode
- High Resistance Poly
- High voltage available - 12/20V*
- Through Passivation Vias for ROIC applications

Process Characteristics

Operating Voltage	5V, 12V*
Substrate Material	P-Type EPI
Drawn Transistor Length	0.6µm
Gate Oxide Thickness	135Å
Contact size	0.5 µm
Via size	0.5 µm
Contacted Gate Pitch	3.9 µm
Top Metal Thickness	675 nm
Contacted Metal Pitch:	
Metal 1	1.5 µm
Metal 2, 3, 4, 5	1.2 µm
Metal Composition	TiN/AlCu/TiN

* 12V gate option in development

Sample Process Options

Option	Mask Layers†
Standard CMOS	14/20
Add Poly/Poly cap	15/21
Add Hi R Poly resistor	16/22
Add 12V gate‡	19/23

† 2 metal / 5 metal

‡ 12V gate option in development. Requires 3+ metal.

Device Characteristics

(All values typical at 25°C)

Standard Transistors

N-Channel	Typical Value	Unit
Vt	0.7	V
Idsat	450	µA/µm
P-Channel	**Typical Value**	**Unit**
Vt	-0.9	V
Idsat	-250	µA/µm

Resistors

	Typical Value	Unit
Poly	25	Ω/sq
Poly2	44	Ω/sq
Hi R Poly	1000	Ω/sq
N-Diffusion	84	Ω/sq
P-Diffusion	112	Ω/sq
N-Well	824	Ω/sq

Capacitors

Poly-Poly	Typical Value	Unit
Area	0.9	fF/µm^2