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LA C3

Process Technology

LA C3: 0.35µm Process Technology

Overview

The LA C3 process family from LA Semiconductor is designed to support medium density, high performance mixed signal designs. Built in the former AMI/onsemi 200mm factory in Pocatello, Idaho, LA C3 offers many of the same features as the onsemi C3 process and is well-suited to extend the lifetime of legacy C3 products. LA C3 is a cost-effective solution for new designs that don’t require leading edge dimensions.

Features

- 3-5 Metal layers
- Poly to Poly Capacitors with improved lifetime
- EEPROM
- Schottky Diode
- High Resistance Poly
- Through Passivation Vias for ROIC applications

Process Characteristics

Operating Voltage	3.3V, 5V*
Substrate Material	P-Type EPI
Drawn Transistor Length	0.35µm
Gate Oxide Thickness	70Å
Contact size	0.4 µm
Via size	0.5 µm
Contacted Gate Pitch	2.9 µm
Top Metal Thickness	675 nm
Contacted Metal Pitch:	
Metal 1	1.1 µm
Metal 2, 3, 4, 5	1.2 µm
Metal Composition	TiN/AlCu/TiN

* 5V gate option in development

Sample Process Options

Option	Mask Layers†
Standard CMOS	17/21
Add Poly/Poly cap	20/24
Add Hi R Poly resistor	21/25
Add 5V gate*	23/27

† 3 metal / 5 metal

* 5V gate option in development

Device Characteristics

(All values typical at 25°C)

Standard Transistors

N-Channel	Typical Value	Unit
Vt	0.5	V
Idsat	510	µA/µm
P-Channel	**Typical Value**	**Unit**
Vt	-0.5	V
Idsat	-260	µA/µm

Resistors

	Typical Value	Unit
Poly	125	Ω/sq
Poly2	45	Ω/sq
Hi R Poly	1000	Ω/sq
N-Diffusion	95	Ω/sq
P-Diffusion	100	Ω/sq
N-Well	1300	Ω/sq

Capacitors

Poly-Poly	Typical Value	Unit
Area	0.947	fF/µm^2